AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device comprising:

a first silicon layer formed on a semiconductor substrate through a gate insulator film with an upper portion and a lower portion larger in width than a central portion for serving as a gate electrode; and

a first silicide film formed on said first silicon layer for serving as said gate electrode, wherein

said first silicon layer serving as said gate electrode includes said upper portion having a reverse mesa shape and said lower portion having a forward mesa shape.

2. (Cancelled)

3. (Original) The semiconductor device according to claim 1, wherein

said first silicon layer includes a lower layer consisting of a polysilicon layer and an upper layer consisting of an amorphous silicon layer.

4. (Original) The semiconductor device according to claim 1, wherein

the width of said lower portion of said first silicon layer is smaller than the width of said upper portion of said first silicon layer.

5. (Original) The semiconductor device according to claim 1, further comprising:

a second silicon layer formed at a prescribed interval from said gate electrode with an upper portion and a lower portion larger in width than a central portion for serving as a wire, and

a second silicide film formed on said second silicon layer for serving as said wire.

6. (Original) The semiconductor device according to claim 5, wherein said first silicon layer and said second silicon layer consist of the same silicon layer.

7. (Original) The semiconductor device according to claim 5, wherein said second silicon layer includes a lower layer consisting of a polysilicon layer and an upper layer consisting of an amorphous silicon layer.

8. (Original) The semiconductor device according to claim 5, wherein the width of said lower portion of said second silicon layer is smaller than the width of said upper portion of said second silicon layer.

9. (Original) The semiconductor device according to claim 1, further comprising:

a second silicon layer formed at a prescribed interval from said gate electrode with an upper portion and a lower potion larger in width than a central portion for serving as a gate electrode, and

a second silicide film formed on said second silicon layer for serving as said gate electrode.

10. (Original) The semiconductor device according to claim 9, wherein said first silicon layer and said second silicon layer consist of the same silicon layer.

11. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate electrode, consisting of a single metal layer, formed on said semiconductor substrate through a gate insulator film with an upper potion and a lower portion larger in width than a central portion, wherein

the gate electrode, consisting of a single metal layer, includes an upper portion having a reverse mesa shape and a lower portion having a forward mesa shape.

12. (Currently Amended) A semiconductor device comprising:

a first conductive layer formed on a semiconductor substrate with an upper potion and a lower portion larger in width than a central portion; and

a second conductive layer formed on said semiconductor substrate at a prescribed interval from said first conductive layer with an upper potion and a lower portion larger in width than a central portion, wherein

the first conductive layer includes an upper portion having a reverse mesa shape and a lower portion having a forward mesa shape.

13. (Original) The semiconductor device according to claim 12, wherein

said first conductive layer and said second conductive layer include:

a silicon layer with an upper potion and a lower portion larger in width than a central portion, and

a silicide film formed on said silicon layer.

14. (Withdrawn) A method of fabricating a semiconductor device comprising steps of:

forming a first silicon layer on a semiconductor layer through a gate insulator film;

forming an etching mask on said first silicon layer;

working said first silicon layer to serve as a gate electrode having an upper portion and a lower portion larger in width than a central portion by etching said first silicon layer through said etching mask serving as a mask; and

forming a first silicide film serving as said gate electrode on said first silicon layer.

15. (Withdrawn) The method of fabricating a semiconductor device according to claim 14, wherein

said step of forming said gate electrode includes:

a first etching step of dry-etching said first silicon layer in a reverse mesa shape with etching gas containing Cl_2, O_2 and HBr, and

a second etching step of dry-etching said first silicon layer in a forward mesa shape with etching gas containing O_2 and HBr after said first etching step.

16. (Withdrawn) The method of fabricating a semiconductor device according to claim 14, wherein

said first silicon layer includes a lower layer consisting of a polysilicon layer and an upper layer consisting of an amorphous silicon layer.

17. (Withdrawn) The method of fabricating a semiconductor device according to claim 14, wherein

the width of said lower portion of said first silicon layer is smaller than the width of said upper portion of said first silicon layer.

18. (Withdrawn) The method of fabricating a semiconductor device according to claim 14, further comprising steps of:

forming a second silicon layer on said semiconductor layer at a prescribed interval from said gate electrode,

forming an etching mask on said second silicon layer,

working said second silicon layer to serve as a wire or a gate electrode having an upper portion and a lower portion larger in width than a central portion by etching said second silicon layer through said etching mask serving as a mask, and

forming a second silicide film serving as said wire or said gate electrode on said second silicon layer.

19. (Withdrawn) The method of fabricating a semiconductor device according to claim 18, forming said first silicon layer and said second silicon layer by patterning the same silicon layer.

20. (Withdrawn) The method of fabricating a semiconductor device according to claim 18, wherein

said second silicon layer includes a lower layer consisting of a polysilicon layer and an upper layer consisting of an amorphous silicon layer.

21. (Withdrawn) The method of fabricating a semiconductor device according to claim 18, wherein

the width of said lower portion of said second silicon layer is smaller than the width of said upper portion of said second silicon layer.

22. (New) A semiconductor device comprising:

a first silicon layer formed on a semiconductor substrate through a gate insulator film with an upper portion and a lower portion larger in width than a central portion for serving as a gate electrode; and

a first silicide film formed on said first silicon layer for serving as said gate electrode, wherein

the width of said lower portion of said first silicon layer is smaller than the width of said upper portion of said first silicon layer.

23. (New) A semiconductor device comprising:

a first silicon layer formed on a semiconductor substrate through a gate insulator film with an upper portion and a lower portion larger in width than a central portion for serving as a gate electrode;

a first silicide film formed on said first silicon layer for serving as said gate electrode;

a second silicon layer formed at a prescribed interval from said gate electrode with an upper portion and a lower portion larger in width than a central portion for serving as a wire; and

a second silicide film formed on said second silicon layer for serving as said wire.

24. (New) The semiconductor device according to claim 23, wherein

said first silicon layer and said second silicon layer consist of the same silicon layer.

25. (New) The semiconductor device according to claim 23, wherein

said second silicon layer includes a lower layer consisting of a polysilicon layer and an upper layer consisting of an amorphous silicon layer.

26. (New) The semiconductor device according to claim 23, wherein

the width of said lower portion of said second silicon layer is smaller than the width of said upper portion of said second silicon layer.